We claim:

1. An optical waveguide on a substrate, where the optical waveguide is comprised of:

a core comprised of monocrystalline silicon, where the core and a silicon body of a transistor are formed from the same layer of monocrystalline silicon on the same substrate,
and
a cladding comprised of a plurality of dielectric materials, where at least one of the plurality of dielectric materials is comprised of a salicide block layer used during the fabrication of a transistor on the same substrate.

2. The optical waveguide of claim 1, wherein the substrate is comprised of a layer of silicon dioxide disposed on a layer of monocrystalline silicon.

3. The optical waveguide of claim 2, wherein the cladding includes a bottom layer comprised of the layer of silicon dioxide, where the silicon dioxide layer is used to electrically isolate the transistor formed on the substrate from the lower layer of monocrystalline silicon.

4. The optical waveguide of claim 1, wherein the substrate is comprised of:

a first layer comprised of monocrystalline silicon,
a second layer comprised of silicon dioxide disposed on the first layer,

a third layer comprised of monocrystalline silicon disposed on the second layer and

a fourth layer comprised of silicon dioxide disposed on the third layer.

5. The optical waveguide of claim 4, wherein the cladding includes a bottom layer comprised of the fourth layer of the substrate, where the fourth layer is used to electrically isolate the transistor formed on the substrate from the third layer.

6. The optical waveguide of claim 1, wherein the substrate is comprised of sapphire.

7. The optical waveguide of claim 1, wherein the substrate is comprised of silicon on nothing, where the waveguide core is formed from the top layer of silicon.

8. The optical waveguide of claim 1, wherein the cladding includes a bottom cladding comprised of the top layer of the substrate.

9. The optical waveguide of claim 1, wherein the cladding includes a layer of dielectric material formed at the same time as the sidewall passivation for the silicon body of a transistor.

10. The optical waveguide of claim 1, wherein the cladding includes a plurality of layers of dielectric material formed at the same time as a plurality of dielectric materials used as a gate spacer for a transistor.

11. The optical waveguide of claim 1, wherein the cladding includes a layer of dielectric material formed at the same time as a contact punch-through layer for a transistor.

12. The optical waveguide of claim 1, wherein the cladding includes a layer of dielectric material formed at the same time as an inter-level dielectric for a transistor.

13. The optical waveguide of claims 9, 10 and 11 wherein the layer of dielectric material included in the cladding is selected from the group comprising: silicon dioxide and silicon nitride.

14. The optical waveguide of claim 1, wherein at least one of the plurality of dielectric materials is selected from a group of dielectrics used at the same time to form a dielectric element of a transistor, the group of dielectrics comprising: a contact punch-through layer, an inter-layer dielectric film, a gate spacer, a salicide block, a dielectric spacer, a sidewall passivation film, an isolation dielectric, an oxide spacer and a field oxide.

15. The optical waveguide of claim 14, wherein thermal oxidation is used to form a sidewall passivation film, where the sidewall passivation film is used as one of a plurality of dielectric materials for the optical waveguide and is formed at the same time as the passivation film for the body of a transistor.

16. The optical waveguide of claim 1, wherein at least one of the plurality of dielectric materials is selected from the group comprising: SiO_2, SiCOH, SiCOF, Si_3N_4, SiON, BPSG and silicon-based materials including one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

17. The optical waveguide of claim 1, wherein the transistor is selected from the group comprising: a CMOS transistor, a BiCMOS transistor, a bipolar junction transistor (BJT) and a junction FET (JFET) transistor.

18. The optical waveguide of claim 1, wherein the salicide block layer is used as a gate spacer during the fabrication of a transistor on the same substrate.

19. An optical waveguide on a substrate, where the optical waveguide is comprised of:

a core comprised of:

a slab of monocrystalline silicon, where the slab and a silicon body of a transistor are formed from the same layer of monocrystalline silicon on the same substrate,

a layer of dielectric material disposed on the slab of monocrystalline silicon, where the layer of dielectric material and a gate oxide for a transistor are formed at the same time of the same dielectric material, and

a strip of polysilicon disposed on the layer of dielectric material, where the strip and a polysilicon gate for a transistor are formed at the same time from the same polysilicon,

and

a cladding comprised of a plurality of dielectric materials, where at least one of the plurality of dielectric materials is comprised of a salicide block layer used during the fabrication of a transistor on the same substrate.

20. The optical waveguide of claim 19, wherein the substrate is comprised of a layer of silicon dioxide disposed on a layer of monocrystalline silicon.

21. The optical waveguide of claim 20, wherein the cladding includes a bottom layer comprised of the layer of silicon dioxide, where the silicon dioxide layer is used to electrically isolate the transistor formed on the substrate from the lower layer of monocrystalline silicon.

22. The optical waveguide of claim 19, wherein the substrate is comprised of:

a first layer comprised of monocrystalline silicon,
a second layer comprised of silicon dioxide disposed on the first layer,
a third layer comprised of monocrystalline silicon disposed on the second layer and
a fourth layer comprised of silicon dioxide disposed on the third layer.

23. The optical waveguide of claim 22, wherein the cladding includes a bottom layer comprised of the fourth layer of the substrate, where the fourth layer is used to electrically isolate the transistor formed on the substrate from the third layer.

24. The optical waveguide of claim 19, wherein the substrate is comprised of sapphire.

25. The optical waveguide of claim 19, wherein the substrate is comprised of silicon on nothing, where the waveguide core is formed from the top layer of silicon.

26. The optical waveguide of claim 19, wherein the cladding includes a bottom cladding comprised of the top layer of the substrate.

27. The optical waveguide of claim 19, wherein the cladding includes a layer of dielectric material formed at the same time as the sidewall f for the silicon body of a transistor.

28. The optical waveguide of claim 19, wherein the cladding includes a plurality of layers of dielectric material formed at the same time as a plurality of dielectric materials used as a gate spacer for a transistor.

29. The optical waveguide of claim 19, wherein the cladding includes a layer of dielectric material formed at the same time as a contact punch-through layer for a transistor.

30. The optical waveguide of claim 19, wherein the cladding includes a layer of dielectric material formed at the same time as an inter-level dielectric for a transistor.

31. The optical waveguide of claims 27, 28 and 29 wherein the layer of dielectric material included in the cladding is selected from the group comprising: silicon dioxide and silicon nitride.

32. The optical waveguide of claim 19, wherein at least one of the plurality of dielectric materials is selected from a group of dielectrics used at the same time to form a dielectric element of a transistor, the group of dielectrics comprising: a contact punch-through layer, an inter-layer dielectric film, a gate spacer, a salicide block, a dielectric spacer, a sidewall passivation film, an isolation dielectric, an oxide spacer and a field oxide.

33. The optical waveguide of claim 14, wherein thermal oxidation is used to form a sidewall passivation film, where the sidewall passivation film is used as one of a plurality of dielectric materials for the optical waveguide and is formed at the same time as the sidewall passivation film for the body of a transistor.

34. The optical waveguide of claim 19, wherein at least one of the plurality of dielectric materials is selected from the group comprising: SiO_2, SiCOH, SiCOF, Si_3N_4, SiON, BPSG and silicon-based materials including

one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

35. The optical waveguide of claim 19, wherein the transistor is selected from the group comprising: a CMOS transistor, a BiCMOS transistor, a bipolar junction transistor (BJT) and a junction FET (JFET) transistor.

36. The optical waveguide of claim 19, wherein the salicide block layer is used as a gate spacer during the fabrication of a transistor on the same substrate.

37. An optical waveguide on a substrate, where the optical waveguide is comprised of:

a core comprised of:

a slab of monocrystalline silicon, where the slab and a silicon body of a transistor are formed from the same layer of monocrystalline silicon on the same substrate,

and

a strip of polysilicon disposed on the slab of monocrystalline silicon, where the strip and a polysilicon gate for a transistor are formed at the same time from the same polysilicon,

and

a cladding comprised of a plurality of dielectric materials,

where at least one of the plurality of dielectric materials is comprised of a salicide block layer used during the fabrication of a transistor.

38. The optical waveguide of claim 37, wherein the substrate is comprised of a layer of silicon dioxide disposed on a layer of monocrystalline silicon.

39. The optical waveguide of claim 38, wherein the cladding includes a bottom layer comprised of the layer of silicon dioxide, where the silicon dioxide layer is used to electrically isolate the transistor formed on the substrate from the lower layer of monocrystalline silicon.

40. The optical waveguide of claim 37, wherein the substrate is comprised of:

a first layer comprised of monocrystalline silicon,
a second layer comprised of silicon dioxide disposed on the first layer,
a third layer comprised of monocrystalline silicon disposed on the second layer and
a fourth layer comprised of silicon dioxide disposed on the third layer.

41. The optical waveguide of claim 40, wherein the cladding includes a bottom layer comprised of the fourth layer of the substrate, where the fourth layer is used to electrically isolate the transistor formed on the substrate from the third layer.

42. The optical waveguide of claim 37, wherein the substrate is comprised of sapphire.

43. The optical waveguide of claim 37, wherein the substrate is comprised of silicon on nothing, where the waveguide core is formed from the top layer of silicon.

44. The optical waveguide of claim 37, wherein the cladding includes a bottom cladding comprised of the top layer of the substrate.

45. The optical waveguide of claim 37, wherein the cladding includes a layer of dielectric material formed at the same time as the sidewall passivation for the silicon body of a transistor.

46. The optical waveguide of claim 37, wherein the cladding includes a plurality of layers of dielectric material formed at the same time as a plurality of dielectric materials used as a gate spacer for a transistor.

47. The optical waveguide of claim 37, wherein the cladding includes a layer of dielectric material formed at the same time as a contact punch-through layer for a transistor.

48. The optical waveguide of claim 37, wherein the cladding includes a layer of dielectric material formed at the same time as an inter-level dielectric for a transistor.

49. The optical waveguide of claims 45, 46 and 47, wherein the layer of dielectric material included in the cladding is selected from the group comprising: silicon dioxide and silicon nitride.

50. The optical waveguide of claim 37, wherein at least one of the plurality of dielectric materials is selected from a group of dielectrics used at the same time to form a dielectric element of a transistor, the group of dielectrics comprising: a contact punch-through layer, an inter-layer dielectric film, a gate spacer, a salicide block, a dielectric spacer, a sidewall passivation film, an isolation dielectric, an oxide spacer and a field oxide.

51. The optical waveguide of claim 50, wherein thermal oxidation is used to form a sidewall passivation film, where the sidewall passivation film is used as one of a plurality of dielectric materials for the optical waveguide and is formed at the same time as the sidewall passivation film for the body of a transistor.

52. The optical waveguide of claim 37, wherein at least one of the plurality of dielectric materials is selected from the group comprising: SiO_2, SiCOH, SiCOF, Si_3N_4, SiON, BPSG and silicon-based materials including one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

53. The optical waveguide of claim 37, wherein the transistor is selected from the group comprising: a CMOS transistor, a BiCMOS transistor, a bipolar junction transistor (BJT) and a junction FET (JFET) transistor.

54. The optical waveguide of claim 37, wherein the salicide block layer is used as a gate spacer during the fabrication of a transistor on the same substrate.

55. An optical waveguide on a substrate, where the optical waveguide is comprised of:

a core comprised of:

a slab of monocrystalline silicon,

a layer of dielectric material disposed on the slab of monocrystalline silicon,

and

a strip of monocrystalline silicon disposed on the layer of dielectric material, where the strip and a silicon body of a transistor are formed from the same monocrystalline silicon on the same substrate,

and

a cladding comprised of a plurality of dielectric materials, where at least one of the plurality of dielectric materials is comprised of a salicide block layer used during the fabrication of a transistor on the same substrate.

56. The optical waveguide of claim 55, wherein the substrate is comprised of:

a first layer comprised of monocrystalline silicon,

a second layer comprised of silicon dioxide disposed on the first layer,

a third layer comprised of monocrystalline silicon disposed on the second layer and

a fourth layer comprised of silicon dioxide disposed on the third layer.

57. The optical waveguide of claim 56, wherein the cladding includes a bottom layer comprised of the fourth layer of the substrate, where the fourth layer is used to electrically isolate the transistor formed on the substrate from the third layer.

58. The optical waveguide of claim 55, wherein the cladding includes a bottom cladding comprised of the top layer of the substrate.

59. The optical waveguide of claim 55, wherein the cladding includes a layer of dielectric material formed at the same time as the sidewall passivation for the silicon body of a transistor.

60. The optical waveguide of claim 55, wherein the cladding includes a plurality of layers of dielectric material formed at the same time as a plurality of dielectric materials used as a gate spacer for a transistor.

61. The optical waveguide of claim 55, wherein the cladding includes a layer of dielectric material formed at the same time as a contact punch-through layer for a transistor.

62. The optical waveguide of claim 55, wherein the cladding includes a layer of dielectric material formed at the same time as an inter-level dielectric for a transistor.

63. The optical waveguide of claims 60, 61 and 62 wherein the layer of dielectric material included in the cladding is selected from the group comprising: silicon dioxide and silicon nitride.

64. The optical waveguide of claim 55, wherein at least one of the plurality of dielectric materials is selected from a group of dielectrics used at the same time to form a dielectric element of a transistor, the group of dielectrics comprising: a contact punch-through layer, an inter-layer dielectric film, a gate spacer, a salicide block, a dielectric spacer, a sidewall passivation film, an isolation dielectric, an oxide spacer and a field oxide.

65. The optical waveguide of claim 64, wherein thermal oxidation is used to form a sidewall passivation film, where the sidewall passivation film is used as one of a plurality of dielectric materials for the optical waveguide and is formed at the same time as the sidewall passivation film for the body of a transistor.

66. The optical waveguide of claim 55, wherein at least one of the plurality of dielectric materials is selected from the group comprising: SiO_2, SiCOH, SiCOF, Si_3N_4, SiON, BPSG and silicon-based materials including one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

67. The optical waveguide of claim 55, wherein the transistor is selected from the group comprising: a CMOS transistor, a BiCMOS transistor, a bipolar junction transistor (BJT) and a junction FET (JFET) transistor.

68. The optical waveguide of claim 55, wherein the salicide block layer is used as a gate spacer during the fabrication of a transistor on the same substrate.

69. A light scattering element for an optical waveguide with a core, where the core of the waveguide is comprised of monocrystalline silicon, and where the core and a silicon body of a transistor are formed from the same layer of monocrystalline silicon on the same substrate,
and
where the light scattering element is comprised of:

a layer of dielectric material disposed on the core, where the layer of dielectric material and a gate oxide for a transistor are formed at the same time of the same dielectric material,
a layer of polysilicon disposed on the layer of dielectric material, where the layer of polysilicon and a polysilicon gate for a transistor are formed at the same time from the same polysilicon,
and
a cladding comprised of a plurality of dielectric materials disposed over:
the core,
the layer of dielectric material and

the layer of polysilicon,

where at least one of the plurality of dielectric materials is comprised of a layer of salicide block used during the fabrication of a transistor.

70. The light scattering element of claim 69, wherein the substrate is comprised of a layer of silicon dioxide disposed on a layer of monocrystalline silicon.

71. The light scattering element of claim 70, wherein the cladding includes a bottom layer comprised of the layer of silicon dioxide, where the silicon dioxide layer is used to electrically isolate the transistor formed on the substrate from the lower layer of monocrystalline silicon.

72. The light scattering element of claim 69, wherein the substrate is comprised of:

a first layer comprised of monocrystalline silicon,
a second layer comprised of silicon dioxide disposed on the first layer,
a third layer comprised of monocrystalline silicon disposed on the second layer and
a fourth layer comprised of silicon dioxide disposed on the third layer.

73. The light scattering element of claim 72, wherein the cladding includes a bottom layer comprised of the fourth layer of the substrate, where the fourth layer is used to electrically isolate the transistor formed on the substrate from the third layer.

74. The light scattering element of claim 69, wherein the substrate is comprised of sapphire.

75. The light scattering element of claim 69, wherein the substrate is comprised of silicon on nothing, where the waveguide core is formed from the top layer of silicon.

76. The light scattering element of claim 69, wherein the cladding includes a bottom cladding comprised of the top layer of the substrate.

77. The light scattering element of claim 69, wherein the cladding includes a layer of dielectric material formed at the same time as the sidewall passivation for the silicon body of a transistor.

78. The light scattering element of claim 69, wherein the cladding includes a plurality of layers of dielectric material formed at the same time as a plurality of dielectric materials used as a gate spacer for a transistor.

79. The light scattering element of claim 69, wherein the cladding includes a layer of dielectric material formed at the same time as a contact punch-through layer for a transistor.

80. The light scattering element of claim 69, wherein the cladding includes a layer of dielectric material formed at the same time as an inter-level dielectric for a transistor.

81. The light scattering element of claims 77, 78 and 79 wherein the layer of dielectric material included in the cladding is selected from the group comprising: silicon dioxide and silicon nitride.

82. The light scattering element of claim 69, wherein at least one of the plurality of dielectric materials is selected from a group of dielectrics used at the same time to form a dielectric element of a transistor, the group of dielectrics comprising: a contact punch-through layer, an inter-layer dielectric film, a gate spacer, a salicide block, a dielectric spacer, a sidewall passivation film, an isolation dielectric, an oxide spacer and a field oxide.

83. The light scattering element of claim 82, wherein thermal oxidation is used to form a sidewall passivation film, where the sidewall passivation film is used as one of a plurality of dielectric materials for the optical waveguide and is formed at the same time as the sidewall passivation film for the body of a transistor.

84. The light scattering element of claim 69, wherein at least one of the plurality of dielectric materials is selected from the group comprising: SiO_2, SiCOH, SiCOF, Si_3N_4, SiON, BPSG and silicon-based materials including one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

85. The light scattering element of claim 69, wherein the transistor is selected from the group comprising: a CMOS transistor, a BiCMOS

transistor, a bipolar junction transistor (BJT) and a junction FET (JFET) transistor.

86. The light scattering element of claim 69, wherein the salicide block layer is used as a gate spacer during the fabrication of a transistor on the same substrate.

87. A light scattering element for an optical waveguide with a core, where the core of the waveguide is comprised of monocrystalline silicon, and where the core and a silicon body of a transistor are formed from the same layer of monocrystalline silicon on the same substrate, and
where the light scattering element is comprised of:
a layer of polysilicon disposed on the core, where the layer of polysilicon and a polysilicon gate for a transistor are formed at the same time from the same polysilicon,
and
a cladding comprised of a plurality of dielectric materials disposed over the core and the layer of polysilicon, where at least one of the plurality of dielectric materials is comprised of a layer of salicide block used during the fabrication of a transistor.

88. The light scattering element of claim 87, wherein the substrate is comprised of a layer of silicon dioxide disposed on a layer of monocrystalline silicon.

89. The light scattering element of claim 88, wherein the cladding includes a bottom layer comprised of the layer of silicon dioxide, where the silicon dioxide layer is used to electrically isolate the transistor formed on the substrate from the lower layer of monocrystalline silicon.

90. The light scattering element of claim 87, wherein the substrate is comprised of:

a first layer comprised of monocrystalline silicon,
a second layer comprised of silicon dioxide disposed on the first layer,
a third layer comprised of monocrystalline silicon disposed on the second layer and
a fourth layer comprised of silicon dioxide disposed on the third layer.

91. The light scattering element of claim 90, wherein the cladding includes a bottom layer comprised of the fourth layer of the substrate, where the fourth layer is used to electrically isolate the transistor formed on the substrate from the third layer.

92. The light scattering element of claim 87, wherein the substrate is comprised of sapphire.

93. The light scattering element of claim 87, wherein the substrate is comprised of silicon on nothing, where the waveguide core is formed from the top layer of silicon.

94. The light scattering element of claim 87, wherein the cladding includes a bottom cladding comprised of the top layer of the substrate.

95. The light scattering element of claim 87, wherein the cladding includes a layer of dielectric material formed at the same time as the sidewall passivation for the silicon body of a transistor.

96. The light scattering element of claim 87, wherein the cladding includes a plurality of layers of dielectric material formed at the same time as a plurality of dielectric materials used as a gate spacer for a transistor.

97. The light scattering element of claim 87, wherein the cladding includes a layer of dielectric material formed at the same time as a contact punch-through layer for a transistor.

98. The light scattering element of claim 87, wherein the cladding includes a layer of dielectric material formed at the same time as an inter-level dielectric for a transistor.

99. The light scattering element of claims 95, 96 and 97, wherein the layer of dielectric material included in the cladding is selected from the group comprising: silicon dioxide and silicon nitride.

100. The light scattering element of claim 87, wherein at least one of the plurality of dielectric materials is selected from a group of dielectrics used at the same time to form a dielectric element of a transistor, the group of

dielectrics comprising: a contact punch-through layer, an inter-layer dielectric film, a gate spacer, a salicide block, a dielectric spacer, a sidewall passivation film, an isolation dielectric, an oxide spacer and a field oxide.

101. The light scattering element of claim 100, wherein thermal oxidation is used to form a sidewall passivation film, where the sidewall passivation film is used as one of a plurality of dielectric materials for the optical waveguide and is formed at the same time as the sidewall passivation film for the body of a transistor.

102. The light scattering element of claim 87, wherein at least one of the plurality of dielectric materials is selected from the group comprising: SiO_2, SiCOH, SiCOF, Si_3N_4, SiON, BPSG and silicon-based materials including one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

103. The light scattering element of claim 87, wherein the transistor is selected from the group comprising: a CMOS transistor, a BiCMOS transistor, a bipolar junction transistor (BJT) and a junction FET (JFET) transistor.

104. The light scattering element of claim 87, wherein the salicide block layer is used as a gate spacer during the fabrication of a transistor on the same substrate.

105. A light scattering element for an optical waveguide with a core, where the core of the optical waveguide is comprised of:

a slab of monocrystalline silicon,

a first layer of dielectric material disposed on the slab of monocrystalline silicon,

and

a strip of monocrystalline silicon disposed on the first layer of dielectric material, where the strip and a silicon body of a transistor are formed from the same monocrystalline silicon on the same substrate,

and

where the light scattering element is comprised of:

a second layer of dielectric material disposed on the strip of monocrystalline silicon, where the second layer of dielectric material and a gate oxide for a transistor are formed at the same time of the same dielectric material,

a layer of polysilicon disposed on the second layer of dielectric material, where the layer of polysilicon and a polysilicon gate for a transistor are formed at the same time from the same polysilicon,

and

a cladding comprised of a plurality of dielectric materials, where the cladding is disposed over

the core,

the second layer of dielectric materials and

the layer of polysilicon, and

where at least one of the cladding layers is comprised of a layer of salicide block used during the fabrication of a transistor.

106. The light scattering element of claim 105, wherein the substrate is comprised of:

a first layer comprised of monocrystalline silicon,
a second layer comprised of silicon dioxide disposed on the first layer,
a third layer comprised of monocrystalline silicon disposed on the second layer and
a fourth layer comprised of silicon dioxide disposed on the third layer.

107. The light scattering element of claim 106, wherein the cladding includes a bottom layer comprised of the fourth layer of the substrate, where the fourth layer is used to electrically isolate the transistor formed on the substrate from the third layer.

108. The light scattering element of claim 105, wherein the cladding includes a bottom cladding comprised of the top layer of the substrate.

109. The light scattering element of claim 105, wherein the cladding includes a layer of dielectric material formed at the same time as the sidewall passivation for the silicon body of a transistor.

110. The light scattering element of claim 105, wherein the cladding includes a plurality of layers of dielectric material formed at the same time as a plurality of dielectric materials used as a gate spacer for a transistor.

111. The light scattering element of claim 105, wherein the cladding includes a layer of dielectric material formed at the same time as a contact punch-through layer for a transistor.

112. The light scattering element of claim 105, wherein the cladding includes a layer of dielectric material formed at the same time as an inter-level dielectric for a transistor.

113. The light scattering element of claims 109, 110 and 111 wherein the layer of dielectric material included in the cladding is selected from the group comprising: silicon dioxide and silicon nitride.

114. The light scattering element of claim 105, wherein at least one of the plurality of dielectric materials is selected from a group of dielectrics used at the same time to form a dielectric element of a transistor, the group of dielectrics comprising: a contact punch-through layer, an inter-layer dielectric film, a gate spacer, a salicide block, a dielectric spacer, a sidewall passivation film, an isolation dielectric, an oxide spacer and a field oxide.

115. The optical waveguide of claim 114, wherein thermal oxidation is used to form a sidewall passivation film, where the sidewall passivation film is used as one of a plurality of dielectric materials for the optical waveguide

and is formed at the same time as the sidewall passivation film for the body of a transistor.

116. The light scattering element of claim 105, wherein at least one of the plurality of dielectric materials is selected from the group comprising: SiO_2, SiCOH, SiCOF, Si_3N_4, SiON, BPSG and silicon-based materials including one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

117. The light scattering element of claim 105, wherein the transistor is selected from the group comprising: a CMOS transistor, a BiCMOS transistor, a bipolar junction transistor (BJT) and a junction FET (JFET) transistor.

118. The light scattering element of claim 105, wherein the salicide block layer is used as a gate spacer during the fabrication of a transistor on the same substrate.

119. A light scattering element for an optical waveguide with a core, where the core of the optical waveguide is comprised of:

a layer of monocrystalline silicon,

a layer of dielectric material disposed on the layer of monocrystalline silicon,

and

a strip of monocrystalline silicon disposed on the layer of dielectric material, where the strip and a silicon body of a transistor are formed from the same monocrystalline silicon on the same substrate,

and

where the light scattering element is comprised of:

a layer of polysilicon disposed on the strip of monocrystalline silicon, where the layer of polysilicon and a polysilicon gate for a transistor are formed at the same time from the same polysilicon,

and

a cladding comprised of a plurality of dielectric materials, where the cladding is disposed over the core and the layer of polysilicon, and where at least one of the cladding layers is comprised of a layer of salicide block used during the fabrication of a transistor.

120. The light scattering element of claim 119, wherein the substrate is comprised of:

a first layer comprised of monocrystalline silicon,

a second layer comprised of silicon dioxide disposed on the first layer,

a third layer comprised of monocrystalline silicon disposed on the second layer and

a fourth layer comprised of silicon dioxide disposed on the third layer.

121. The light scattering element of claim 120, wherein the cladding includes a bottom layer comprised of the fourth layer of the substrate, where

the fourth layer is used to electrically isolate the transistor formed on the substrate from the third layer.

122. The light scattering element of claim 119, wherein the cladding includes a bottom cladding comprised of the top layer of the substrate.

123. The light scattering element of claim 119, wherein the cladding includes a layer of dielectric material formed at the same time as the sidewall passivation for the silicon body of a transistor.

124. The light scattering element of claim 119, wherein the cladding includes a plurality of layers of dielectric material formed at the same time as a plurality of dielectric materials used as a gate spacer for a transistor.

125. The light scattering element of claim 119, wherein the cladding includes a layer of dielectric material formed at the same time as a contact punch-through layer for a transistor.

126. The light scattering element of claim 119, wherein the cladding includes a layer of dielectric material formed at the same time as an inter-level dielectric for a transistor.

127. The light scattering element of claims 123, 124 and 125, wherein the layer of dielectric material included in the cladding is selected from the group comprising: silicon dioxide and silicon nitride.

128. The light scattering element of claim 119, wherein at least one of the plurality of dielectric materials is selected from a group of dielectrics used at the same time to form a dielectric element of a transistor, the group of dielectrics comprising: a contact punch-through layer, an inter-layer dielectric film, a gate spacer, a salicide block, a dielectric spacer, a sidewall passivation film, an isolation dielectric, an oxide spacer and a field oxide.

129. The light scattering element of claim 128, wherein thermal oxidation is used to form a sidewall passivation film, where the sidewall passivation film is used as one of a plurality of dielectric materials for the optical waveguide and is formed at the same time as the sidewall passivation film for the body of a transistor.

130. The light scattering element of claim 119, wherein at least one of the plurality of dielectric materials is selected from the group comprising: SiO_2, SiCOH, SiCOF, Si_3N_4, SiON, BPSG and silicon-based materials including one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

131. The light scattering element of claim 119, wherein the transistor is selected from the group comprising: a CMOS transistor, a BiCMOS transistor, a bipolar junction transistor (BJT) and a junction FET (JFET) transistor.

132. The light scattering element of claim 119, wherein the salicide block layer is used as a gate spacer during the fabrication of a transistor on the same substrate.

133. A light scattering element for an optical waveguide with a core, where the core is comprised of monocrystalline silicon, and where the core and a silicon body of a transistor are formed from the same monocrystalline silicon on the same substrate,
and
where the light scattering element is comprised of:
a structure formed in the core of the optical waveguide,
and
a cladding comprised of a plurality of dielectric materials,
where the cladding is disposed over the core and the structure, and where at least one of the plurality of dielectric materials is comprised of a layer of salicide block used during the fabrication of a transistor.

134. The light scattering element of claim 133, wherein the substrate is comprised of a layer of silicon dioxide disposed on a layer of monocrystalline silicon.

135. The light scattering element of claim 134, wherein the cladding includes a bottom layer comprised of the layer of silicon dioxide, where the silicon dioxide layer is used to electrically isolate the transistor formed on the substrate from the lower layer of monocrystalline silicon.

136. The light scattering element of claim 133, wherein the substrate is comprised of:

a first layer comprised of monocrystalline silicon,
a second layer comprised of silicon dioxide disposed on the first layer,
a third layer comprised of monocrystalline silicon disposed on the second layer and
a fourth layer comprised of silicon dioxide disposed on the third layer.

137. The light scattering element of claim 136, wherein the cladding includes a bottom layer comprised of the fourth layer of the substrate, where the fourth layer is used to electrically isolate the transistor formed on the substrate from the third layer.

138. The light scattering element of claim 133, wherein the substrate is comprised of sapphire.

139. The light scattering element of claim 133, wherein the substrate is comprised of silicon on nothing, where the waveguide core is formed from the top layer of silicon.

140. The light scattering element of claim 133, wherein the cladding includes a bottom cladding comprised of the top layer of the substrate.

141. The light scattering element of claim 133, wherein the cladding includes a layer of dielectric material formed at the same time as the sidewall passivation for the silicon body of a transistor.

142. The light scattering element of claim 133, wherein the cladding includes a plurality of layers of dielectric material formed at the same time as a plurality of dielectric materials used as a gate spacer for a transistor.

143. The light scattering element of claim 133, wherein the cladding includes a layer of dielectric material formed at the same time as a contact punch-through layer for a transistor.

144. The light scattering element of claim 133, wherein the cladding includes a layer of dielectric material formed at the same time as an inter-level dielectric for a transistor.

145. The light scattering element of claims 141, 142 and 143, wherein the layer of dielectric material included in the cladding is selected from the group comprising: silicon dioxide and silicon nitride.

146. The light scattering element of claim 133, wherein at least one of the plurality of dielectric materials is selected from a group of dielectrics used at the same time to form a dielectric element of a transistor, the group of dielectrics comprising: a contact punch-through layer, an inter-layer dielectric film, a gate spacer, a salicide block, a dielectric spacer, a sidewall passivation film, an isolation dielectric, an oxide spacer and a field oxide.

147. The light scattering element of claim 146, wherein thermal oxidation is used to form a sidewall passivation film, where the sidewall passivation film is used as one of a plurality of dielectric materials for the optical waveguide and is formed at the same time as the sidewall passivation film for the body of a transistor.

148. The light scattering element of claim 133, wherein at least one of the plurality of dielectric materials is selected from the group comprising: SiO_2, SiCOH, SiCOF, Si_3N_4, SiON, BPSG and silicon-based materials including one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

149. The light scattering element of claim 133, wherein the transistor is selected from the group comprising: a CMOS transistor, a BiCMOS transistor, a bipolar junction transistor (BJT) and a junction FET (JFET) transistor.

150. The light scattering element of claim 133, wherein the salicide block layer is used as a gate spacer during the fabrication of a transistor on the same substrate.

151. A light scattering element for a strip loaded optical waveguide, where the core of the waveguide is comprised of:

a slab of monocrystalline silicon on a substrate, where the slab and a silicon body of a transistor are formed from the same monocrystalline silicon on the same substrate,

a layer of a first dielectric material disposed on the slab of monocrystalline silicon, where the layer of a first dielectric material and a gate oxide for a transistor are formed at the same time of the same dielectric material,

and

a strip of polysilicon disposed on the layer of first dielectric material, where the strip of polysilicon and a polysilicon gate for a transistor are formed at the same time from the same polysilicon,

and where the light scattering element is comprised of:

a structure formed in the core of the optical waveguide

and

a cladding comprised of a plurality of dielectric materials,

where the cladding is disposed over the core and the structure, where at least one of the plurality of dielectric materials is comprised of a layer of salicide block used during the fabrication of a transistor.

152. The light scattering element of claim 151, wherein the substrate is comprised of a layer of silicon dioxide disposed on a layer of monocrystalline silicon.

153. The light scattering element of claim 152, wherein the cladding includes a bottom layer comprised of the layer of silicon dioxide, where the

silicon dioxide layer is used to electrically isolate the transistor formed on the substrate from the lower layer of monocrystalline silicon.

154. The light scattering element of claim 151, wherein the substrate is comprised of:

a first layer comprised of monocrystalline silicon,
a second layer comprised of silicon dioxide disposed on the first layer,
a third layer comprised of monocrystalline silicon disposed on the second layer and
a fourth layer comprised of silicon dioxide disposed on the third layer.

155. The light scattering element of claim 154, wherein the cladding includes a bottom layer comprised of the fourth layer of the substrate, where the fourth layer is used to electrically isolate the transistor formed on the substrate from the third layer.

156. The light scattering element of claim 151, wherein the substrate is comprised of sapphire.

157. The light scattering element of claim 151, wherein the substrate is comprised of silicon on nothing, where the waveguide core is formed from the top layer of silicon.

158. The light scattering element of claim 151, wherein the cladding includes a bottom cladding comprised of the top layer of the substrate.

159. The light scattering element of claim 151, wherein the cladding includes a layer of dielectric material formed at the same time as the sidewall passivation for the silicon body of a transistor.

160. The light scattering element of claim 151, wherein the cladding includes a plurality of layers of dielectric material formed at the same time as a plurality of dielectric materials used as a gate spacer for a transistor.

161. The light scattering element of claim 151, wherein the cladding includes a layer of dielectric material formed at the same time as a contact punch-through layer for a transistor.

162. The light scattering element of claim 151, wherein the cladding includes a layer of dielectric material formed at the same time as an inter-level dielectric for a transistor.

163. The light scattering element of claims 159, 160 and 161, wherein the layer of dielectric material included in the cladding is selected from the group comprising: silicon dioxide and silicon nitride.

164. The light scattering element of claim 151, wherein at least one of the plurality of dielectric materials is selected from a group of dielectrics used at the same time to form a dielectric element of a transistor, the group of dielectrics comprising: a contact punch-through layer, an inter-layer

dielectric film, a gate spacer, a salicide block, a dielectric spacer, a sidewall passivation film, an isolation dielectric, an oxide spacer and a field oxide.

165. The light scattering element of claim 164, wherein thermal oxidation is used to form a sidewall passivation film, where the sidewall passivation film is used as one of a plurality of dielectric materials for the optical waveguide and is formed at the same time as the sidewall passivation film for the body of a transistor.

166. The light scattering element of claim 151, wherein at least one of the plurality of dielectric materials is selected from the group comprising: SiO_2, SiCOH, SiCOF, Si_3N_4, SiON, BPSG and silicon-based materials including one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

167. The light scattering element of claim 151, wherein the transistor is selected from the group comprising: a CMOS transistor, a BiCMOS transistor, a bipolar junction transistor (BJT) and a junction FET (JFET) transistor.

168. The light scattering element of claim 151, wherein the salicide block layer is used as a gate spacer during the fabrication of a transistor on the same substrate.

169. A light scattering element for a strip loaded optical waveguide, where the core of the waveguide is comprised of:

a slab of monocrystalline silicon on a substrate, where the slab and a silicon body of a transistor are formed from the same monocrystalline silicon on the same substrate,

and

a strip of polysilicon disposed on the slab of monocrystalline silicon, where the strip of polysilicon and a polysilicon gate for a transistor are formed at the same time from the same polysilicon,

and where the light scattering element is comprised of:

a structure formed in the core of the optical waveguide

and

a cladding comprised of a plurality of dielectric materials,

where the cladding is disposed over the core and the trench, where at least one of the plurality of dielectric materials is comprised of a layer of salicide block used during the fabrication of a transistor.

170. The light scattering element of claim 169, wherein the substrate is comprised of a layer of silicon dioxide disposed on a layer of monocrystalline silicon.

171. The light scattering element of claim 170, wherein the cladding includes a bottom layer comprised of the layer of silicon dioxide, where the silicon dioxide layer is used to electrically isolate the transistor formed on the substrate from the lower layer of monocrystalline silicon.

172. The light scattering element of claim 169, wherein the substrate is comprised of:

a first layer comprised of monocrystalline silicon,
a second layer comprised of silicon dioxide disposed on the first layer,
a third layer comprised of monocrystalline silicon disposed on the second layer and
a fourth layer comprised of silicon dioxide disposed on the third layer.

173. The light scattering element of claim 172, wherein the cladding includes a bottom layer comprised of the fourth layer of the substrate, where the fourth layer is used to electrically isolate the transistor formed on the substrate from the third layer.

174. The light scattering element of claim 169, wherein the substrate is comprised of sapphire.

175. The light scattering element of claim 169, wherein the substrate is comprised of silicon on nothing, where the waveguide core is formed from the top layer of silicon.

176. The light scattering element of claim 169, wherein the cladding includes a bottom cladding comprised of the top layer of the substrate.

177. The light scattering element of claim 169, wherein the cladding includes a layer of dielectric material formed at the same time as the sidewall passivation for the silicon body of a transistor.

178. The light scattering element of claim 169, wherein the cladding includes a plurality of layers of dielectric material formed at the same time as a plurality of dielectric materials used as a gate spacer for a transistor.

179. The light scattering element of claim 169, wherein the cladding includes a layer of dielectric material formed at the same time as a contact punch-through layer for a transistor.

180. The light scattering element of claim 169, wherein the cladding includes a layer of dielectric material formed at the same time as an inter-level dielectric for a transistor.

181. The light scattering element of claims 177, 178 and 179, wherein the layer of dielectric material included in the cladding is selected from the group comprising: silicon dioxide and silicon nitride.

182. The light scattering element of claim 169, wherein at least one of the plurality of dielectric materials is selected from a group of dielectrics used at the same time to form a dielectric element of a transistor, the group of dielectrics comprising: a contact punch-through layer, an inter-layer dielectric film, a gate spacer, a salicide block, a dielectric spacer, a sidewall passivation film, an isolation dielectric, an oxide spacer and a field oxide.

183. The light scattering element of claim 182, wherein thermal oxidation is used to form a sidewall passivation film, where the sidewall passivation film is used as one of a plurality of dielectric materials for the optical

waveguide and is formed at the same time as the sidewall passivation film for the body of a transistor.

184. The light scattering element of claim 169, wherein at least one of the plurality of dielectric materials is selected from the group comprising: SiO_2, SiCOH, SiCOF, Si_3N_4, SiON, BPSG and silicon-based materials including one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

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185. The light scattering element of claim 169, wherein the transistor is selected from the group comprising: a CMOS transistor, a BiCMOS transistor, a bipolar junction transistor (BJT) and a junction FET (JFET) transistor.

186. The light scattering element of claim 169, wherein the salicide block layer is used as a gate spacer during the fabrication of a transistor on the same substrate.

187. A light scattering element for a strip loaded optical waveguide, where the core of the waveguide is comprised of:

a slab of monocrystalline silicon on a substrate, where the slab and a silicon body of a transistor are formed from the same monocrystalline silicon on the same substrate,

a layer of first dielectric material disposed on the slab of monocrystalline silicon, where the layer of first dielectric material and

a gate oxide for a transistor are formed at the same time of the same dielectric material,

and

a strip of polysilicon disposed on the layer of first dielectric material, where the strip of polysilicon and a polysilicon gate for a transistor are formed at the same time from the same polysilicon,

and where the light scattering element is comprised of:

a structure formed in the core of the optical waveguide,

and

a cladding comprised of a plurality of dielectric materials,

where the cladding is disposed over the core and the trench, where at least one of the plurality of dielectric materials is comprised of a layer of salicide block used during the fabrication of a transistor.

188. The light scattering element of claim 187, wherein the substrate is comprised of a layer of silicon dioxide disposed on a layer of monocrystalline silicon.

189. The light scattering element of claim 188, wherein the cladding includes a bottom layer comprised of the layer of silicon dioxide, where the silicon dioxide layer is used to electrically isolate the transistor formed on the substrate from the lower layer of monocrystalline silicon.

190. The light scattering element of claim 187, wherein the substrate is comprised of:

a first layer comprised of monocrystalline silicon,
a second layer comprised of silicon dioxide disposed on the first layer,
a third layer comprised of monocrystalline silicon disposed on the second layer and
a fourth layer comprised of silicon dioxide disposed on the third layer.

191. The light scattering element of claim 190, wherein the cladding includes a bottom layer comprised of the fourth layer of the substrate, where the fourth layer is used to electrically isolate the transistor formed on the substrate from the third layer.

192. The light scattering element of claim 187, wherein the substrate is comprised of sapphire.

193. The light scattering element of claim 187, wherein the substrate is comprised of silicon on nothing, where the waveguide core is formed from the top layer of silicon.

194. The light scattering element of claim 187, wherein the cladding includes a bottom cladding comprised of the top layer of the substrate.

195. The light scattering element of claim 187, wherein the cladding includes a layer of dielectric material formed at the same time as the sidewall passivation for the silicon body of a transistor.

196. The light scattering element of claim 187, wherein the cladding includes a plurality of layers of dielectric material formed at the same time as a plurality of dielectric materials used as a gate spacer for a transistor.

197. The light scattering element of claim 187, wherein the cladding includes a layer of dielectric material formed at the same time as a contact punch-through layer for a transistor.

198. The light scattering element of claim 187, wherein the cladding includes a layer of dielectric material formed at the same time as an inter-level dielectric for a transistor.

199. The light scattering element of claims 195, 196 and 197 wherein the layer of dielectric material included in the cladding is selected from the group comprising: silicon dioxide and silicon nitride.

200. The light scattering element of claim 187, wherein at least one of the plurality of dielectric materials is selected from a group of dielectrics used at the same time to form a dielectric element of a transistor, the group of dielectrics comprising: a contact punch-through layer, an inter-layer dielectric film, a gate spacer, a salicide block, a dielectric spacer, a sidewall passivation film, an isolation dielectric, an oxide spacer and a field oxide.

201. The light scattering element of claim 200, wherein thermal oxidation is used to form a sidewall passivation film, where the sidewall passivation film is used as one of a plurality of dielectric materials for the optical

waveguide and is formed at the same time as the sidewall passivation film for the body of a transistor.

202. The light scattering element of claim 187, wherein at least one of the plurality of dielectric materials is selected from the group comprising: SiO_2, SiCOH, SiCOF, Si_3N_4, SiON, BPSG and silicon-based materials including one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

203. The light scattering element of claim 187, wherein the transistor is selected from the group comprising: a CMOS transistor, a BiCMOS transistor, a bipolar junction transistor (BJT) and a junction FET (JFET) transistor.

204. The light scattering element of claim 187, wherein the salicide block layer is used as a gate spacer during the fabrication of a transistor on the same substrate.

205. A light scattering element for a strip loaded optical waveguide, where the core of the waveguide is comprised of:

a slab of monocrystalline silicon on a substrate, where the slab and a silicon body of a transistor are formed from the same monocrystalline silicon on the same substrate,

and

a strip of polysilicon disposed on the slab of monocrystalline silicon, where the strip of polysilicon and a polysilicon gate for a transistor are formed at the same time from the same polysilicon,

and where the light scattering element is comprised of:

a structure formed in slab of monocrystalline silicon in the core of the optical waveguide,

and

a cladding comprised of a plurality of dielectric materials,

where the cladding is disposed over the core and the trench, where at least one of the plurality of dielectric materials is comprised of a layer of salicide block used during the fabrication of a transistor.

206. The light scattering element of claim 205, wherein the substrate is comprised of a layer of silicon dioxide disposed on a layer of monocrystalline silicon.

207. The light scattering element of claim 206, wherein the cladding includes a bottom layer comprised of the layer of silicon dioxide, where the silicon dioxide layer is used to electrically isolate the transistor formed on the substrate from the lower layer of monocrystalline silicon.

208. The light scattering element of claim 205, wherein the substrate is comprised of:

a first layer comprised of monocrystalline silicon,

a second layer comprised of silicon dioxide disposed on the first layer,

a third layer comprised of monocrystalline silicon disposed on the second layer and

a fourth layer comprised of silicon dioxide disposed on the third layer.

209. The light scattering element of claim 208, wherein the cladding includes a bottom layer comprised of the fourth layer of the substrate, where the fourth layer is used to electrically isolate the transistor formed on the substrate from the third layer.

210. The light scattering element of claim 205, wherein the substrate is comprised of sapphire.

211. The light scattering element of claim 205, wherein the substrate is comprised of silicon on nothing, where the waveguide core is formed from the top layer of silicon.

212. The light scattering element of claim 205, wherein the cladding includes a bottom cladding comprised of the top layer of the substrate.

213. The light scattering element of claim 205, wherein the cladding includes a layer of dielectric material formed at the same time as the sidewall passivation for the silicon body of a transistor.

214. The light scattering element of claim 205, wherein the cladding includes a plurality of layers of dielectric material formed at the same time as a plurality of dielectric materials used as a gate spacer for a transistor.

215. The light scattering element of claim 205, wherein the cladding includes a layer of dielectric material formed at the same time as a contact punch-through layer for a transistor.

216. The light scattering element of claim 205, wherein the cladding includes a layer of dielectric material formed at the same time as an inter-level dielectric for a transistor.

217. The light scattering element of claims 213, 214 and 215, wherein the layer of dielectric material included in the cladding is selected from the group comprising: silicon dioxide and silicon nitride.

218. The light scattering element of claim 205, wherein at least one of the plurality of dielectric materials is selected from a group of dielectrics used at the same time to form a dielectric element of a transistor, the group of dielectrics comprising: a contact punch-through layer, an inter-layer dielectric film, a gate spacer, a salicide block, a dielectric spacer, a sidewall passivation film, an isolation dielectric, an oxide spacer and a field oxide.

219. The light scattering element of claim 218, wherein thermal oxidation is used to form a sidewall passivation film, where the sidewall passivation film is used as one of a plurality of dielectric materials for the optical waveguide and is formed at the same time as the sidewall passivation film for the body of a transistor.

220. The light scattering element of claim 205, wherein at least one of the plurality of dielectric materials is selected from the group comprising: SiO_2, SiCOH, SiCOF, Si_3N_4, SiON, BPSG and silicon-based materials including one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

221. The light scattering element of claim 205, wherein the transistor is selected from the group comprising: a CMOS transistor, a BiCMOS transistor, a bipolar junction transistor (BJT) and a junction FET (JFET) transistor.

222. The light scattering element of claim 205, wherein the salicide block layer is used as a gate spacer during the fabrication of a transistor on the same substrate.

223. A light scattering element for an optical waveguide on a substrate, where the substrate is comprised of:

a first layer comprised of monocrystalline silicon,

a second layer comprised of silicon dioxide disposed on the first layer,

a third layer comprised of monocrystalline silicon disposed on the second layer,

a fourth layer comprised of silicon dioxide disposed on the third layer, and

a fifth layer comprised of monocrystalline silicon disposed on the fourth layer,

where the core of the waveguide is comprised of the third, fourth and fifth layers,
and where the light scattering element is comprised of:
a structure formed substantially in the fifth layer of the substrate
and
a cladding comprised of a plurality of dielectric materials,
where the cladding is disposed over the core and the trench, where at least one of the plurality of dielectric materials is comprised of a layer of salicide block used during the fabrication of a transistor.

224. The light scattering element of claim 223, wherein the substrate is comprised of:

a first layer comprised of monocrystalline silicon,
a second layer comprised of silicon dioxide disposed on the first layer,
a third layer comprised of monocrystalline silicon disposed on the second layer and
a fourth layer comprised of silicon dioxide disposed on the third layer.

225. The light scattering element of claim 224, wherein the cladding includes a bottom layer comprised of the fourth layer of the substrate, where the fourth layer is used to electrically isolate the transistor formed on the substrate from the third layer.

226. The light scattering element of claim 223, wherein the cladding includes a bottom cladding comprised of the top layer of the substrate.

227. The light scattering element of claim 223, wherein the cladding includes a layer of dielectric material formed at the same time as the sidewall passivation for the silicon body of a transistor.

228. The light scattering element of claim 223, wherein the cladding includes a plurality of layers of dielectric material formed at the same time as a plurality of dielectric materials used as a gate spacer for a transistor.

229. The light scattering element of claim 223, wherein the cladding includes a layer of dielectric material formed at the same time as a contact punch-through layer for a transistor.

230. The light scattering element of claim 223, wherein the cladding includes a layer of dielectric material formed at the same time as an inter-level dielectric for a transistor.

231. The light scattering element of claims 227, 228 and 229, wherein the layer of dielectric material included in the cladding is selected from the group comprising: silicon dioxide and silicon nitride.

232. The light scattering element of claim 223, wherein at least one of the plurality of dielectric materials is selected from a group of dielectrics used at the same time to form a dielectric element of a transistor, the group of dielectrics comprising: a contact punch-through layer, an inter-layer

dielectric film, a gate spacer, a salicide block, a dielectric spacer, a sidewall passivation film, an isolation dielectric, an oxide spacer and a field oxide.

233. The light scattering element of claim 232, wherein thermal oxidation is used to form a sidewall passivation film, where the sidewall passivation film is used as one of a plurality of dielectric materials for the optical waveguide and is formed at the same time as the sidewall passivation film for the body of a transistor.

234. The light scattering element of claim 223, wherein at least one of the plurality of dielectric materials is selected from the group comprising: SiO_2, SiCOH, SiCOF, Si_3N_4, SiON, BPSG and silicon-based materials including one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

235. The light scattering element of claim 223, wherein the transistor is selected from the group comprising: a CMOS transistor, a BiCMOS transistor, a bipolar junction transistor (BJT) and a junction FET (JFET) transistor.

236. The light scattering element of claim 223, wherein the salicide block layer is used as a gate spacer during the fabrication of a transistor on the same substrate.

237. An active waveguide on a substrate comprising:
a waveguide core comprising:

a slab of monocrystalline silicon on a substrate, where the slab and a silicon body of a transistor are formed from the same monocrystalline silicon on the same substrate,

a layer of a first dielectric material disposed on the slab of monocrystalline silicon, where the layer of a first dielectric material and a gate oxide for a transistor are formed at the same time of the same dielectric material,

and

a strip of polysilicon disposed on the layer of first dielectric material, where the strip of polysilicon and a polysilicon gate for a transistor are formed at the same time from the same polysilicon,

a cladding comprised of a plurality of dielectric materials, where at least one of the plurality of dielectric materials is comprised of a salicide block layer used during the fabrication of a transistor,

a plurality of doped regions in the slab of monocrystalline silicon, where at least one of the plurality of doped regions is doped at the same time with the same dopant as a doped region in the structure of a transistor on the same substrate,

a plurality of ohmic contacts, each of which is formed in a region of the plurality of doped regions in the slab of monocrystalline silicon, where at least one of the plurality of ohmic contacts is formed at the same time with the same material as an ohmic contact in the structure of a transistor on the same substrate,

and

a plurality of conductive plugs coupling each of the plurality of ohmic contacts to at least one of a plurality of metal layers of an integrated circuit, where at least one of the plurality of conductive plugs is formed at the same time with the same material as a conductive plug coupling an ohmic contact of a transistor on the same substrate with the same one of a plurality of metal layers.

238. The active waveguide of claim 237, wherein the substrate is comprised of a layer of silicon dioxide disposed on a layer of monocrystalline silicon.

239. The active waveguide of claim 238, wherein the cladding includes a bottom layer comprised of the layer of silicon dioxide, where the silicon dioxide layer is used to electrically isolate the transistor formed on the substrate from the lower layer of monocrystalline silicon.

240. The active waveguide of claim 237, wherein the substrate is comprised of:

a first layer comprised of monocrystalline silicon,
a second layer comprised of silicon dioxide disposed on the first layer,
a third layer comprised of monocrystalline silicon disposed on the second layer and
a fourth layer comprised of silicon dioxide disposed on the third layer.

241. The active waveguide of claim 240, wherein the cladding includes a bottom layer comprised of the fourth layer of the substrate, where the fourth layer is used to electrically isolate the transistor formed on the substrate from the third layer.

242. The active waveguide of claim 237, wherein the substrate is comprised of sapphire.

243. The active waveguide of claim 237, wherein the substrate is comprised of silicon on nothing, where the waveguide core is formed from the top layer of silicon.

244. The active waveguide of claim 237, wherein the cladding includes a bottom cladding comprised of the top layer of the substrate.

245. The active waveguide of claim 237, wherein the cladding includes a layer of dielectric material formed at the same time as the sidewall passivation for the silicon body of a transistor.

246. The active waveguide of claim 237, wherein the cladding includes a plurality of layers of dielectric material formed at the same time as a plurality of dielectric materials used as a gate spacer for a transistor.

247. The active waveguide of claim 237, wherein the cladding includes a layer of dielectric material formed at the same time as a contact punch-through layer for a transistor.

248. The active waveguide of claim 237, wherein the cladding includes a layer of dielectric material formed at the same time as an inter-level dielectric for a transistor.

249. The active waveguide of claims 245, 246 and 247, wherein the layer of dielectric material included in the cladding is selected from the group comprising: silicon dioxide and silicon nitride.

250. The active waveguide of claim 237, wherein at least one of the plurality of dielectric materials is selected from a group of dielectrics used at the same time to form a dielectric element of a transistor, the group of dielectrics comprising: a contact punch-through layer, an inter-layer dielectric film, a gate spacer, a salicide block, a dielectric spacer, a sidewall passivation film, an isolation dielectric, an oxide spacer and a field oxide.

251. The active waveguide of claim 250, wherein thermal oxidation is used to form a sidewall passivation film, where the sidewall passivation film is used as one of a plurality of dielectric materials for the optical waveguide and is formed at the same time as the sidewall passivation film for the body of a transistor.

252. The active waveguide of claim 237, wherein at least one of the plurality of dielectric materials is selected from the group comprising: SiO_2, SiCOH, SiCOF, Si_3N_4, SiON, BPSG and silicon-based materials including

one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

253. The active waveguide of claim 237, wherein the transistor is selected from the group comprising: a CMOS transistor, a BiCMOS transistor, a bipolar junction transistor (BJT) and a junction FET (JFET) transistor.

254. The active waveguide of claim 237, wherein the salicide block layer is used as a gate spacer during the fabrication of a transistor on the same substrate.

255. The active waveguide of claim 237, wherein an ohmic contact is comprised of a metal silicide.

256. The active waveguide of claim 237, wherein a conductive plug is comprised of tungsten.

257. The active waveguide of claim 237, further comprising fabrication of a local interconnection between a pair of transistors, at the same time as fabricating a local interconnection for coupling an ohmic contact on the slab of monocrystalline silicon with an ohmic contact on a transistor.

258. The active waveguide of claim 257, wherein the local interconnection is comprised of a material selected from the group comprising: tungsten and aluminum.

259. An active waveguide on a substrate comprising:

a waveguide core comprising:

a layer of monocrystalline silicon disposed on the substrate,

a layer of a first dielectric material on the layer of monocrystalline silicon, and

a slab of monocrystalline silicon on the layer of the first dielectric material, where the slab and a silicon body of a transistor are formed from the same monocrystalline silicon on the same substrate,

a cladding comprised of a plurality of dielectric materials, where at least one of the plurality of dielectric materials is comprised of a salicide block layer used during the fabrication of a transistor,

a plurality of doped regions in the slab of monocrystalline silicon, where at least one of the plurality of doped regions is doped at the same time with the same dopant as a doped region in the structure of a transistor on the same substrate,

a plurality of ohmic contacts, each of which is formed in a region of the plurality of doped regions in the slab of monocrystalline silicon, where at least one of the plurality of ohmic contacts is formed at the same time with the same material as an ohmic contact in the structure of a transistor on the same substrate,

and

a plurality of conductive plugs coupling each of the plurality of ohmic contacts to at least one of a plurality of metal layers of an integrated circuit,

where at least one of the plurality of conductive plugs is formed at the same time with the same material as a conductive plug coupling an ohmic contact of a transistor on the same substrate with the same one of a plurality of metal layers.

260. The active waveguide of claim 259, wherein the substrate is comprised of:

a first layer comprised of monocrystalline silicon,
a second layer comprised of silicon dioxide disposed on the first layer,
a third layer comprised of monocrystalline silicon disposed on the second layer and
a fourth layer comprised of silicon dioxide disposed on the third layer.

261. The active waveguide of claim 260, wherein the cladding includes a bottom layer comprised of the fourth layer of the substrate, where the fourth layer is used to electrically isolate the transistor formed on the substrate from the third layer.

262. The active waveguide of claim 259, wherein the cladding includes a bottom cladding comprised of the top layer of the substrate.

263. The active waveguide of claim 259, wherein the cladding includes a layer of dielectric material formed at the same time as the sidewall passivation for the silicon body of a transistor.

264. The active waveguide of claim 259, wherein the cladding includes a plurality of layers of dielectric material formed at the same time as a plurality of dielectric materials used as a gate spacer for a transistor.

265. The active waveguide of claim 259, wherein the cladding includes a layer of dielectric material formed at the same time as a contact punch-through layer for a transistor.

266. The active waveguide of claim 259, wherein the cladding includes a layer of dielectric material formed at the same time as an inter-level dielectric for a transistor.

267. The active waveguide of claims 263, 264 and 265, wherein the layer of dielectric material included in the cladding is selected from the group comprising: silicon dioxide and silicon nitride.

268. The active waveguide of claim 259, wherein at least one of the plurality of dielectric materials is selected from a group of dielectrics used at the same time to form a dielectric element of a transistor, the group of dielectrics comprising: a contact punch-through layer, an inter-layer dielectric film, a gate spacer, a salicide block, a dielectric spacer, a sidewall passivation film, an isolation dielectric, an oxide spacer and a field oxide.

269. The active waveguide of claim 268, wherein thermal oxidation is used to form a sidewall passivation film, where the sidewall passivation film is used as one of a plurality of dielectric materials for the optical waveguide

and is formed at the same time as the sidewall passivation film for the body of a transistor.

270. The active waveguide of claim 259, wherein at least one of the plurality of dielectric materials is selected from the group comprising: SiO_2, SiCOH, SiCOF, Si_3N_4, SiON, BPSG and silicon-based materials including one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

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271. The active waveguide of claim 259, wherein the transistor is selected from the group comprising: a CMOS transistor, a BiCMOS transistor, a bipolar junction transistor (BJT) and a junction FET (JFET) transistor.

272. The active waveguide of claim 259, wherein the salicide block layer is used as a gate spacer during the fabrication of a transistor on the same substrate.

273. The active waveguide of claim 259, wherein an ohmic contact is comprised of a metal silicide.

274. The active waveguide of claim 259, wherein a conductive plug is comprised of tungsten.

275. The active waveguide of claim 259, further comprising fabrication of a local interconnection between a pair of transistors, at the same time as

fabricating a local interconnection for coupling an ohmic contact on the slab of monocrystalline silicon with an ohmic contact on a transistor.

276. The active waveguide of claim 275, wherein the local interconnection is comprised of a material selected from the group comprising: tungsten and aluminum.

277. A waveguide coupling on a substrate, where the waveguide coupling is comprised of:

a core comprised of:

a slab of monocrystalline silicon, with a bidirectional port and a terminating end opposite the bidirectional port, where the slab of silicon and a silicon body of a transistor are formed from the same layer of monocrystalline silicon on the same substrate, and

a slab of polysilicon disposed on top of a portion of the slab of monocrystalline silicon, with a bidirectional port and a terminating end opposite the bidirectional port, where the slab of polysilicon and a polysilicon gate for a transistor are formed at the same time from the same polysilicon,

and

a cladding comprised of a plurality of dielectric materials, where at least one of the plurality of dielectric materials is comprised of a salicide block layer used during the fabrication of a transistor on the same substrate.

278. The waveguide coupling of claim 277, wherein the substrate is comprised of a layer of silicon dioxide disposed on a layer of monocrystalline silicon.

279. The waveguide coupling of claim 278, wherein the cladding includes a bottom layer comprised of the layer of silicon dioxide, where the silicon dioxide layer is used to electrically isolate the transistor formed on the substrate from the lower layer of monocrystalline silicon.

280. The waveguide coupling of claim 277, wherein the substrate is comprised of:

a first layer comprised of monocrystalline silicon,
a second layer comprised of silicon dioxide disposed on the first layer,
a third layer comprised of monocrystalline silicon disposed on the second layer and
a fourth layer comprised of silicon dioxide disposed on the third layer.

281. The waveguide coupling of claim 280, wherein the cladding includes a bottom layer comprised of the fourth layer of the substrate, where the fourth layer is used to electrically isolate the transistor formed on the substrate from the third layer.

282. The waveguide coupling of claim 277, wherein the substrate is comprised of sapphire.

283. The waveguide coupling of claim 277, wherein the substrate is comprised of silicon on nothing, where the waveguide core is formed from the top layer of silicon.

284. The waveguide coupling of claim 277, wherein the cladding includes a bottom cladding comprised of the top layer of the substrate.

285. The waveguide coupling of claim 277, wherein the cladding includes a layer of dielectric material formed at the same time as the sidewall passivation for the silicon body of a transistor.

286. The waveguide coupling of claim 277, wherein the cladding includes a plurality of layers of dielectric material formed at the same time as a plurality of dielectric materials used as a gate spacer for a transistor.

287. The waveguide coupling of claim 277, wherein the cladding includes a layer of dielectric material formed at the same time as a contact punch-through layer for a transistor.

288. The waveguide coupling of claim 277, wherein the cladding includes a layer of dielectric material formed at the same time as an inter-level dielectric for a transistor.

289. The waveguide coupling of claims 285, 286 and 287, wherein the layer of dielectric material included in the cladding is selected from the group comprising: silicon dioxide and silicon nitride.

290. The waveguide coupling of claim 277, wherein at least one of the plurality of dielectric materials is selected from a group of dielectrics used at the same time to form a dielectric element of a transistor, the group of dielectrics comprising: a contact punch-through layer, an inter-layer dielectric film, a gate spacer, a salicide block, a dielectric spacer, a sidewall passivation film, an isolation dielectric, an oxide spacer and a field oxide.

291. The waveguide coupling of claim 290, wherein thermal oxidation is used to form a sidewall passivation film, where the sidewall passivation film is used as one of a plurality of dielectric materials for the waveguide coupling and is formed at the same time as the sidewall passivation film for the body of a transistor.

292. The waveguide coupling of claim 277, wherein at least one of the plurality of dielectric materials is selected from the group comprising: SiO_2, SiCOH, SiCOF, Si_3N_4, SiON, BPSG and silicon-based materials including one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

293. The waveguide coupling of claim 277, wherein the transistor is selected from the group comprising: a CMOS transistor, a BiCMOS transistor, a bipolar junction transistor (BJT) and a junction FET (JFET) transistor.

294. The waveguide coupling of claim 277, wherein the salicide block layer is used as a gate spacer during the fabrication of a transistor on the same substrate.

295. A method for designing a plurality of metal and dielectric layers for an optoelectronic integrated circuit, comprising the steps of:

determining the required electrical and optical properties of the plurality of metal and dielectric layers,
selecting each of the plurality of metal and dielectric layers in accordance with the required electrical and optical properties,
modeling the electrical and optical properties of the selected plurality of metal and dielectric layers in accordance with the required electrical and optical properties,
comparing the results of the modeling step to the required electrical and optical properties of the determining step,
and
repeating the steps of selecting, modeling and comparing until the required electrical and optical properties of the plurality of metal and dielectric layers have been substantially complied with.

296. The method of claim 295, wherein the integrated circuit is fabricated on a substrate, where the substrate is selected from the group comprising: silicon on insulator (SOI), silicon on sapphire (SOS) and a silicon membrane (also known as silicon on nothing, SON).

297. The method of claim 295, wherein the integrated circuit is fabricated using a CMOS fabrication process.

298. The method of claim 295, wherein a transistor is fabricated on the integrated circuit, where the transistor is selected from the group comprising: a CMOS transistor, a BiCMOS transistor, a bipolar junction transistor (BJT) and a junction FET (JFET) transistor.

299. The method of claim 295, wherein at least one of the plurality of dielectric layers is selected from a group of dielectrics used at the same time to form a dielectric element of a transistor, the group of dielectrics comprising: a contact punch-through layer, an inter-layer dielectric film, a gate spacer, a salicide block, a dielectric spacer, a sidewall passivation film, an isolation dielectric, an oxide spacer and a field oxide.

300. The method of claim 295, wherein an optical device is fabricated on the integrated circuit, where the optical device includes at least one of a plurality of dielectric materials.

301. The method of claim 300, wherein at least one of the plurality of dielectric materials is selected from the group comprising: SiO_2, SiCOH, SiCOF, Si_3N_4, SiON, BPSG and silicon-based materials including one or more of the following elements: oxygen, carbon, nitrogen, hydrogen, boron, phosphorus, fluorine and arsenic.

302. A method for fabricating integrated optical devices in a CMOS process with foundry design rules having a minimum feature size, comprising the step of:

designing elements of integrated optical devices with a feature size substantially smaller than the minimum feature size.

303. A method for fabricating integrated optical devices in a CMOS process with foundry design rules having a plurality of x and y geometrical design rules pertaining to the layout of elements along the x and y axes, comprising the step of:

designing elements of integrated optical devices with curved features substantially different than the plurality of x and y geometrical design rules.